

FIG. 1

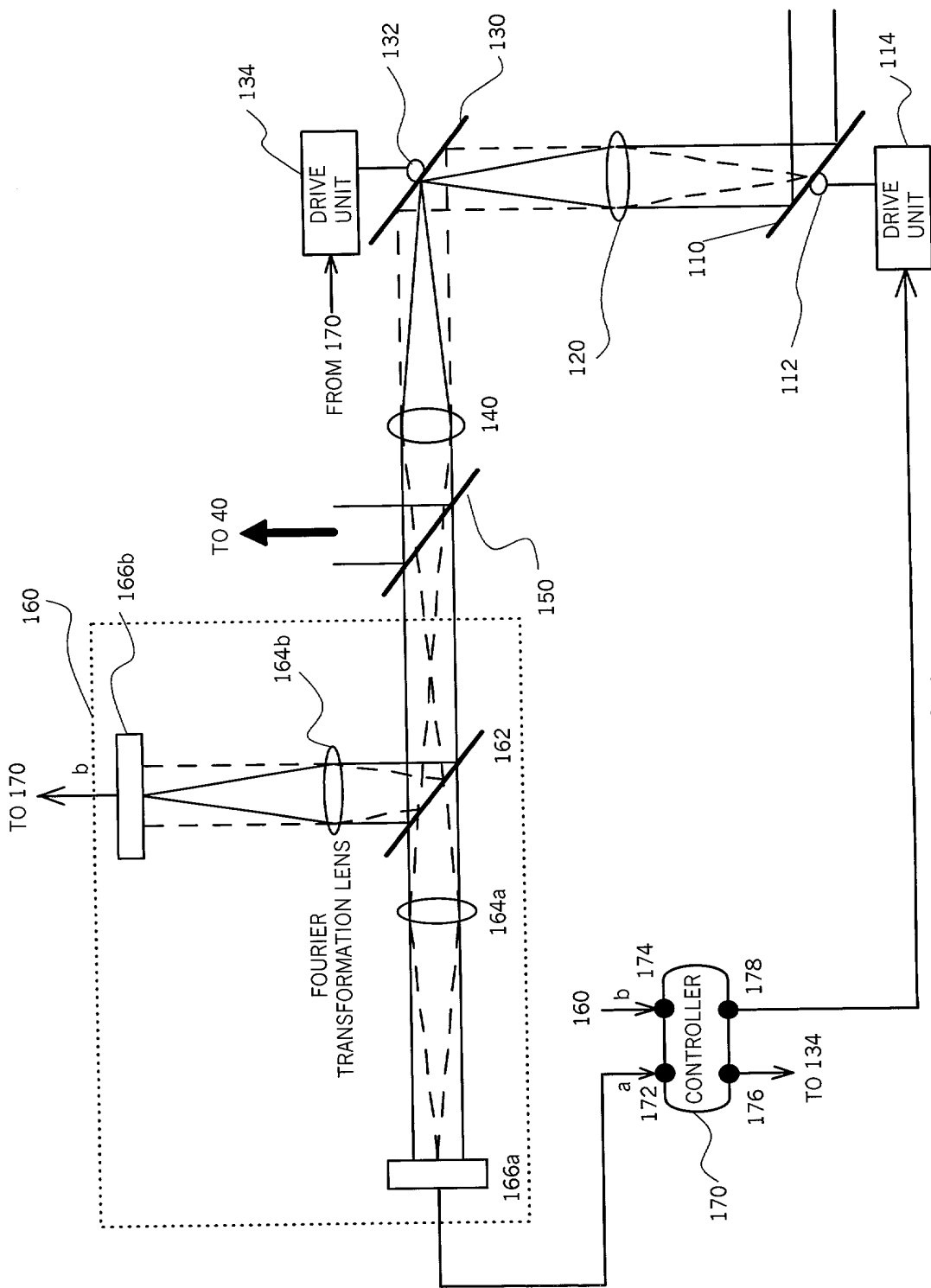


FIG. 2

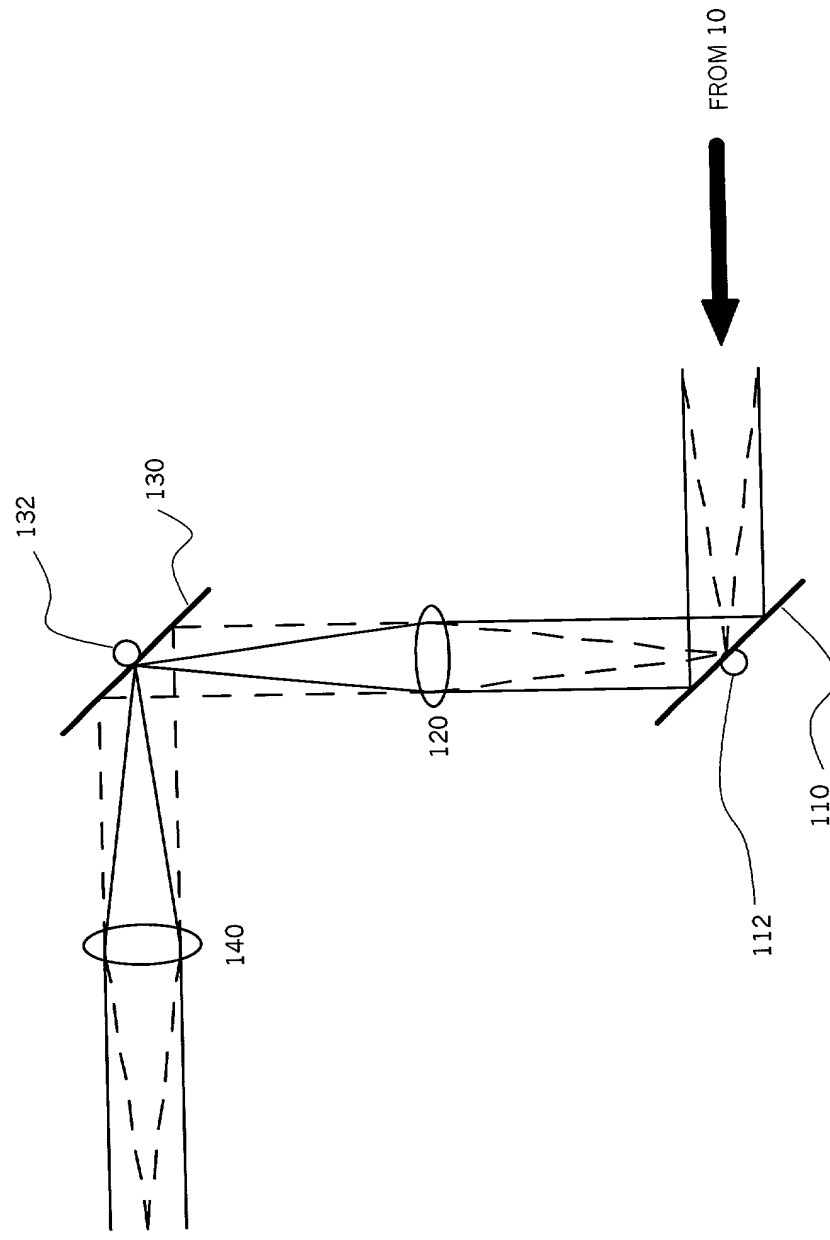


FIG. 3

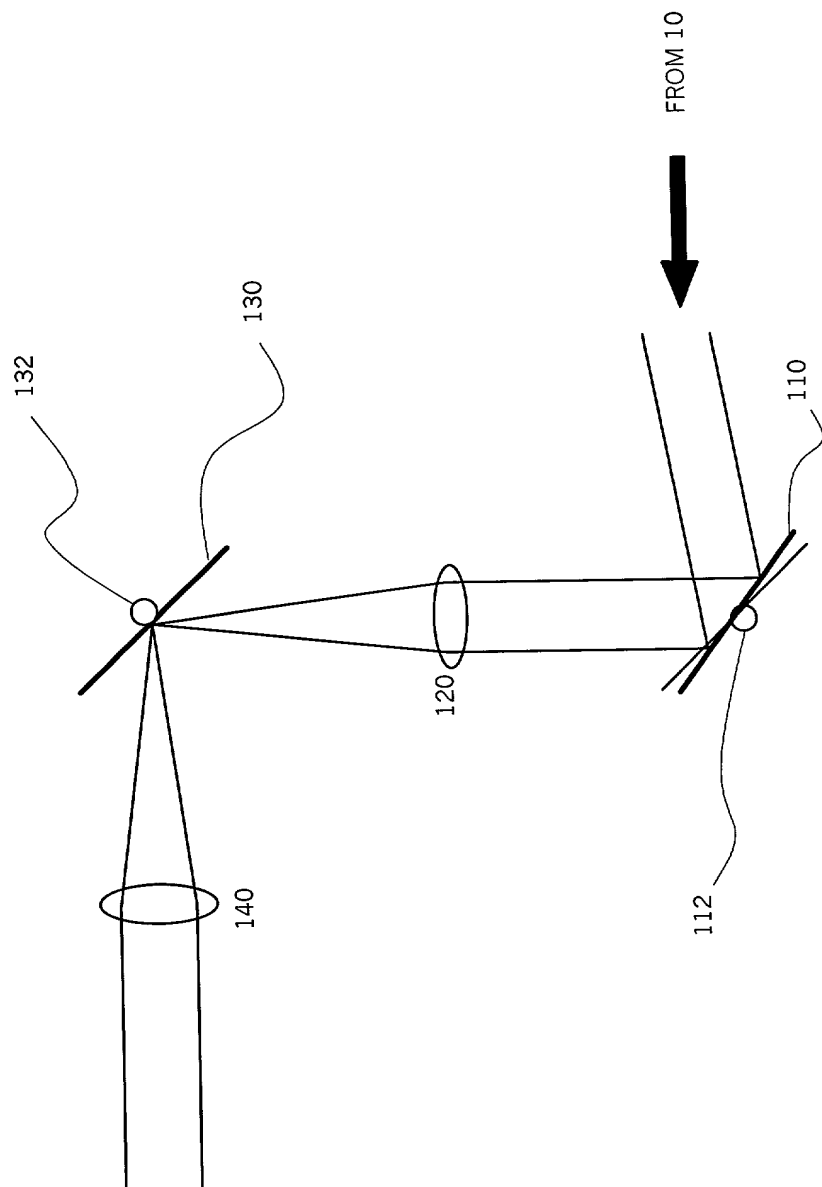


FIG. 4

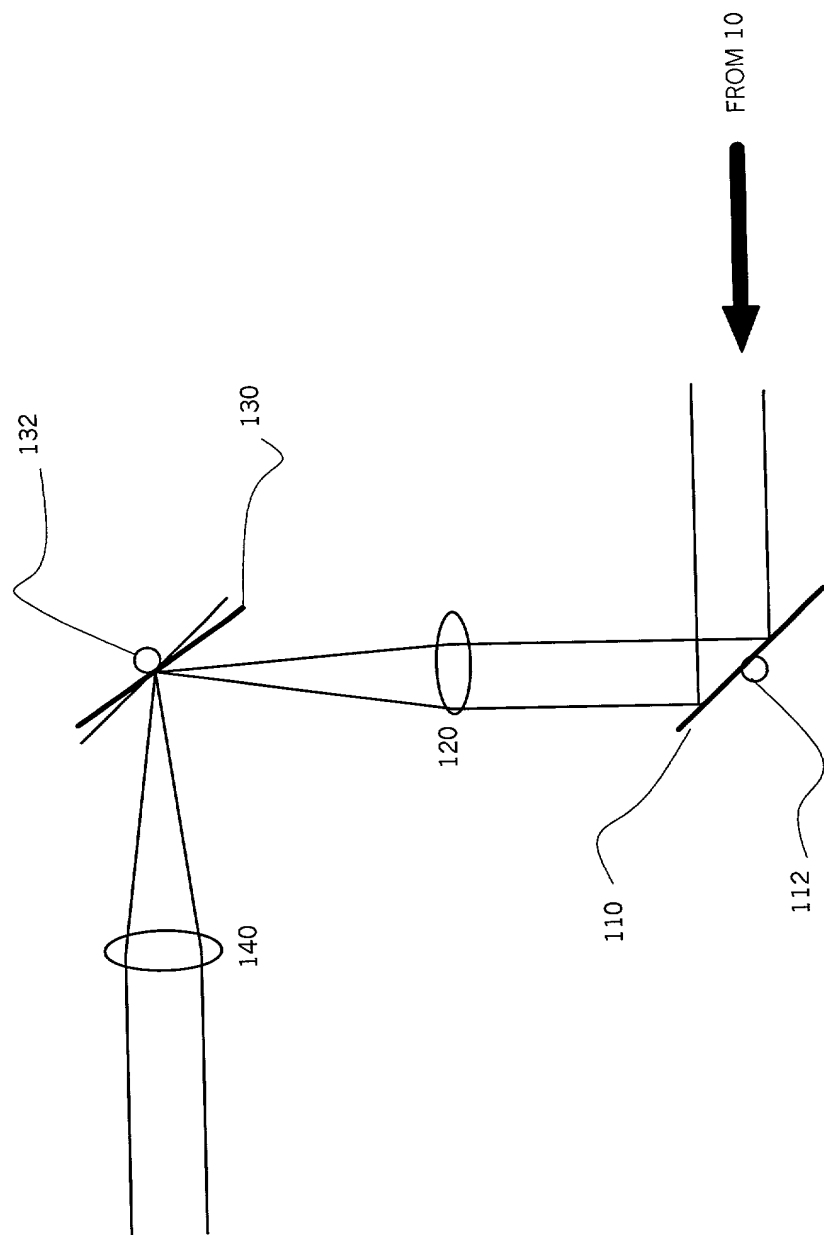


FIG. 5

```
graph TD
    A[CIRCUIT DESIGN] -- "(STEP1)" --> B[MASK FABRICATION]
    B -- "(STEP2)" --> D[WEFER PROCESS  
(PRETREATMENT)]
    C[WEFER MAKING] -- "(STEP3)" --> D
    D -- "(STEP4)" --> E[ASSEMBLY  
(POSTTREATMENT)]
    E -- "(STEP5)" --> F[INSPECTION]
    F -- "(STEP6)" --> G[SHIPPING]
    G -- "(STEP7)" --> H[ ]
```

FIG. 6

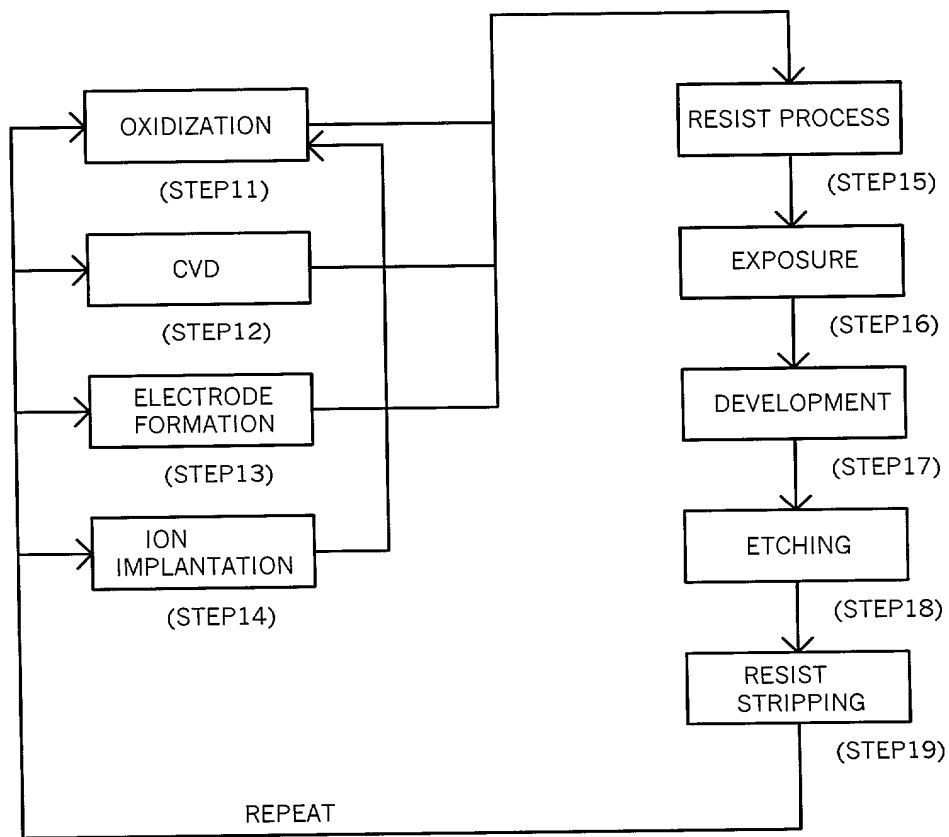


FIG. 7

2003-03-10

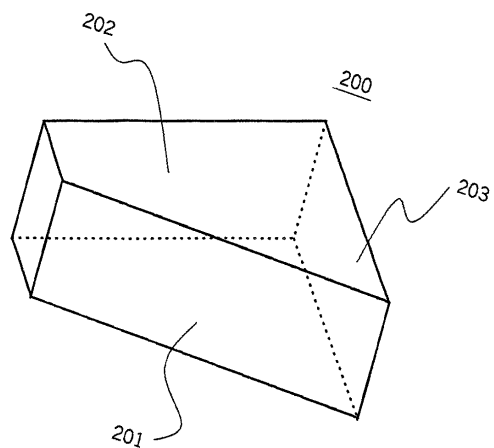


FIG. 8A

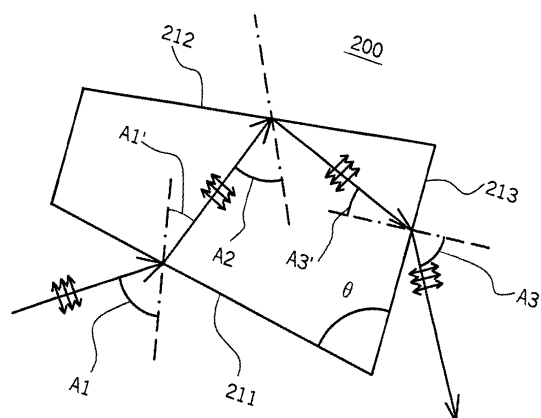


FIG. 8B



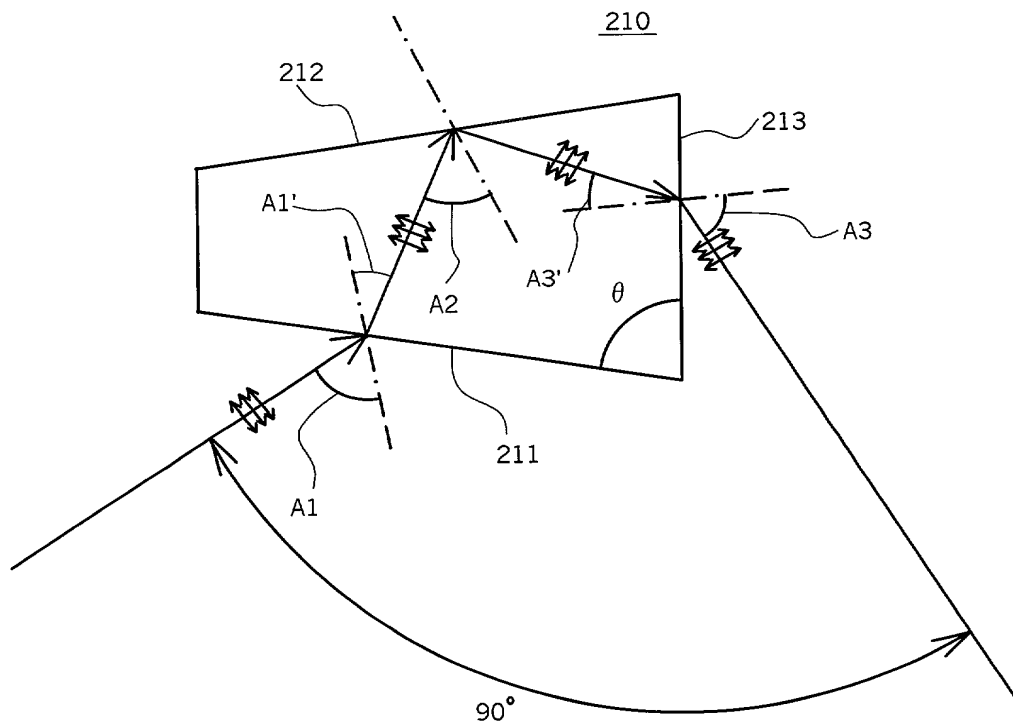


FIG. 9

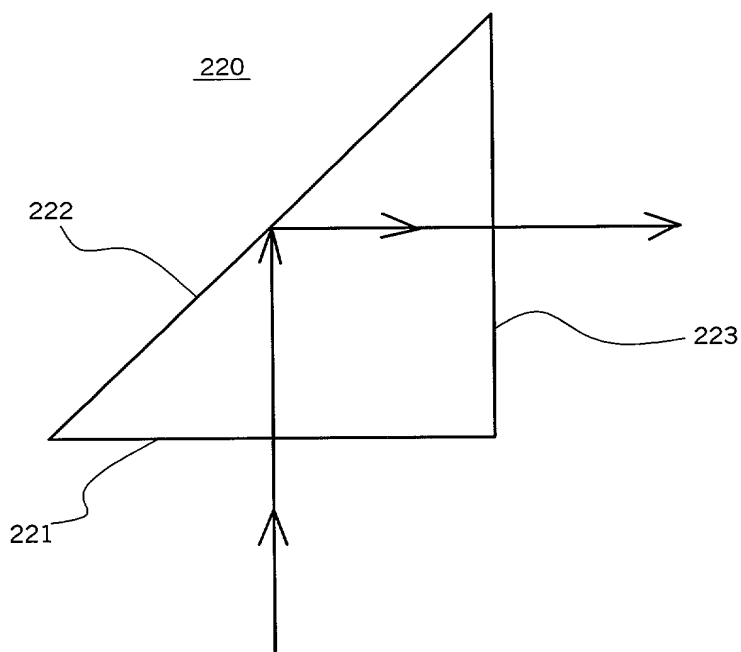


FIG. 10

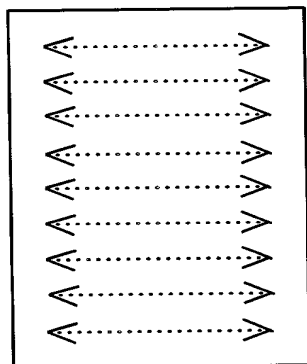


FIG. 11

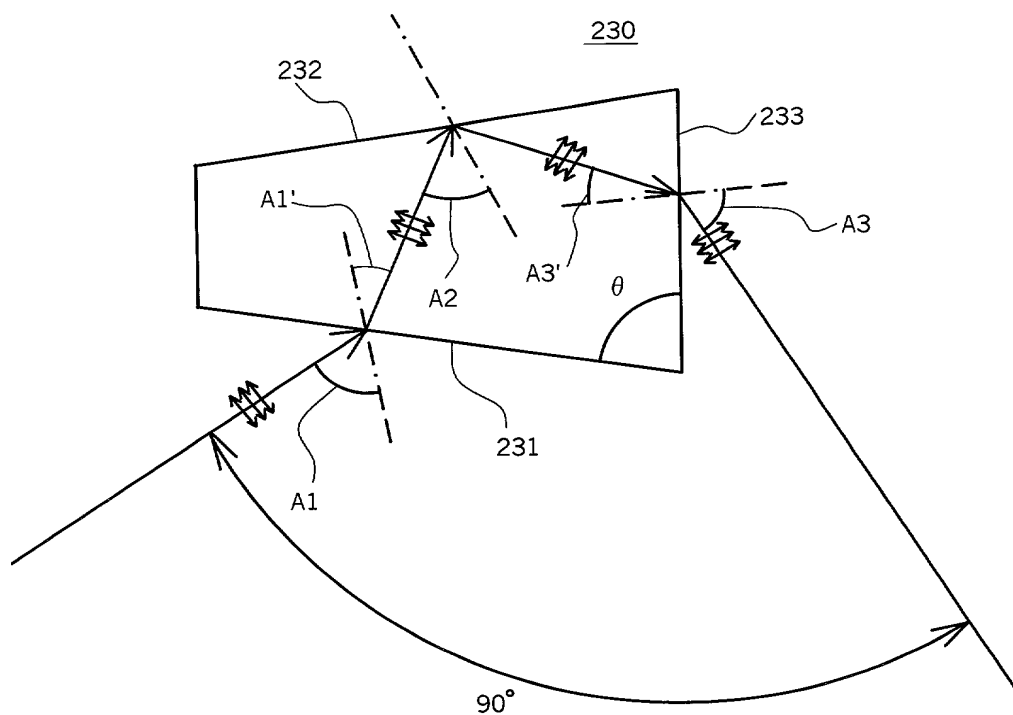


FIG. 12

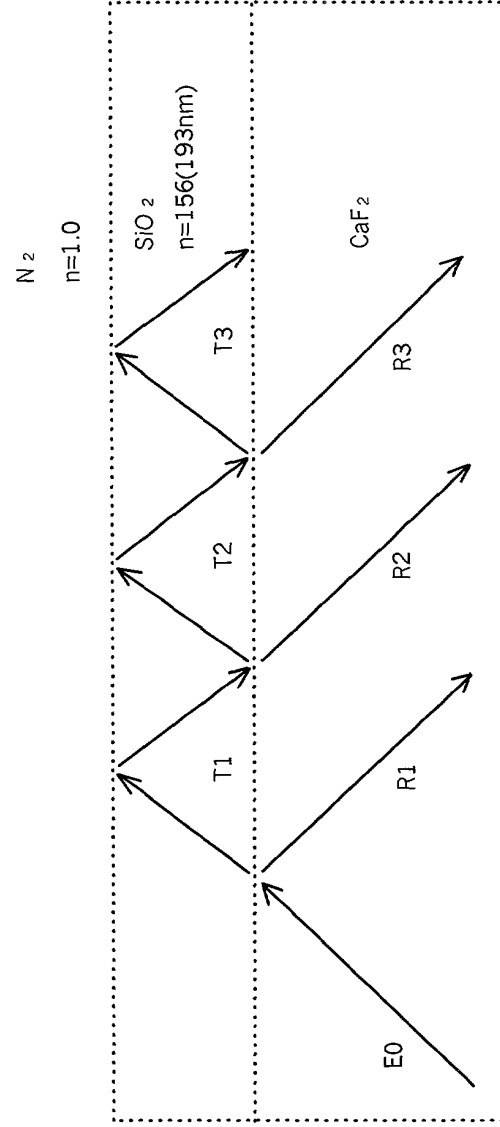


FIG. 13